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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/024,724	12/21/2001	Michael D. Haines	219.40853X00	5908

7590 11/03/2004

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EXAMINER	
WILLIAMS, ALEXANDER O	
ART UNIT	**PAPER NUMBER**
2826	

DATE MAILED: 11/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding..

Office Action Summary	Application No.	Applicant(s)	
	10/024,724	HAINES, MICHAEL D.	
	Examiner	Art Unit	
	Alexander O Williams	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) *29 and 30* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Serial Number: 10/024724 Attorney's Docket #: 219.40853X00
Filing Date: 12/21/01;

Applicant: Haines

Examiner: Alexander Williams

Applicant's Response filed 8/2/04 to election of Group I (claims 1 to 28) in Paper # 14, filed 10/21/03, has been acknowledged.

This application contains claims 29 and 30 drawn to an invention non-elected with traverse in Paper No. 14.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 22, 24 and 26 to 28 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Morris (U.S. Patent # 6,507,101 B1) in view of Jensen et al. (U.S. Patent Application Publication # 2003/0037943 A1).

22. Morris (figures 1A to 4B) specifically figure 2 show an electronic package with protection from electrostatic discharge events comprising: a substrate **210**; a semiconductor die **212** mounted on the substrate; a heat sink **206** in heat conducting relation with the semiconductor die on a side of the semiconductor die opposite the substrate; and a gasket of a lossy material **202** on the substrate surrounding the semiconductor die to protect the die from electromagnetic signals (EMI). Morris fail to explicitly show a gasket to protecting devices from electrostatic discharge pulses. However, it is well know in the art that a gasket protecting from electromagnetic signal can also protect from electrostatic discharge pulses.

Jensen et al. is cited for showing a perforated EMI gasket. Specifically, Jensen et al. (figures 1 to 16) specifically figure 12 discloses a gasket **35** to protecting devices from electrostatic discharge pulses **(see paragraph [0047])** for the purpose of preventing gaps developed to cause a device to fail EMI or ESD requirements.

24. The electronic package according to claim 22, the combination with Morris show wherein the lossy material of the gasket is a static dissipative material having, a volume resistivity of greater than 102 ohm cm.

26. The combination with Morris show wherein the gasket **22** has a hole therein the size of the die through which the die protrudes.

27. The combination with Morris show wherein the gasket has a shielding effectiveness to protect the die from at least 4 kV of electrostatic discharge pulse at a system level in which the electronic package.

28. The combination with Morris show wherein the gasket material has a shielding effectiveness of greater than 45 dB up to 3 GHz.

Therefore, it would have been obvious to one of ordinary skill in the art to use Jensen et al. EMI/ESD gasket to modify Morris EMI gasket for the purpose of preventing gaps developed to cause a device to fail EMI or ESD requirements.

Claims 1, 3 to 8, 11, 12, 22 to 24, 27 and 28 are rejected under 35 U.S.C. § 102(b) as being anticipated by Barker, III et al. (U.S. Patent # 5,175,613) in view of Medolia et al. (U.S. Patent # 5,717,577).

1. Barker, III et al. (figures 1 and 2) specifically figure 2 show an assembly for packaging and cooling a semiconductor die comprising: a substrate **12**; a semiconductor die **24** mounted on the substrate; a thermal spreader **52** in heat conducting relation with the semiconductor die on a side of the die opposite the substrate; and a gasket of a conductive material **26** on the substrate surrounding the die to protect the die from electrostatic discharge pulses.

22. Barker, III et al. (figures 1 and 2) specifically figure 2 show an electronic package with protection from electrostatic discharge events comprising: a substrate **12**; a semiconductor die **24** mounted on the substrate; a heat sink **14** in heat conducting relation with the semiconductor die on a side of the semiconductor die opposite the substrate; and a gasket of a conductive material **26** on the substrate surrounding the semiconductor die to protect the die from electrostatic discharge pulses.

US-PAT-NO: 5175613

DOCUMENT-IDENTIFIER: US 5175613 A

TITLE: Package for EMI, ESD, thermal, and mechanical shock protection of circuit chips

DATE-ISSUED: December 29, 1992

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Barker, III; Charles R.	Harvard	MA	N/A	N/A
Casabona; Richard J.	Stow	MA	N/A	N/A
Fenwick; David M.	Chelmsford	MA	N/A	N/A

(4) In the past, various attempts have been made to provide solutions to each of the above issues individually, but not in combination with one another. For example, heat sinks have long been used for electronics packaging to maintain the temperature of the electronics within their operating range. However, these do not provide shock, EMI, or ESD protection. Similarly, module shielding techniques, such as can found in a TV, VCR, or video decoder, for example, employ a metal "can" that is formed around a series of components, and is connected to provide EMI shielding for the components, but no thermal or mechanical shock protection for the same.

(6) It is therefore the object of the present invention to provide **an integral package for integrated circuits which will protect the circuits from extreme** temperatures, mechanical shock, EMI, and, **ESD**, and also, **shield the environment from EMI emissions from the circuits**.

(9) **For ESD protection**, an additional conductive coating is necessary. This is provided by applying an insulating material to the outside surface of the heat sink, and then applying an additional conductive coating on top of the layer of insulating material. This conductive coating is electrically connected to the heat sink, and to the wiring board reference plane by a conductive gasket, or contact, that is disposed in the heat sink/base interface when the package is assembled.

DETAILED DESCRIPTION:
(1) DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

(5) Also disposed on top surface 22, and generally around its periphery, is a narrow rectangular frame shaped conductive metal strip 25, on top of which is disposed, a similar shaped strip of conductive material 26, which surrounds the mounting area for chips 24. Conductive material 26 is preferably compliant, and can be a spring metal, or conductive elastomer, for example. This acts as an electrical gasket for the interface between heat sink 14 and base 12, and will be discussed in further detail below. A plurality of apertures 28 are disposed in compliant strip 26 at its corners that also pass through board 16 to receive mounting screws or bolts for attaching heat sink 14 to base 12.

Baker, III et al. fail to explicitly show a gasket of a lossy material. However, Baker, III et al. discloses an electrical gasket to protect the die from electrostatic discharges.

Mendolia et al. is cited for showing a gasketed shield that can be shielding emissions of electromagnetic energy. Specifically, Mendolia et al. (figures 1 to 2F) specifically figure 2A discloses a gasket **240** of a lossy material on the substrate **100** surrounding the semiconductor die **120** to protect the die from electrostatic discharge pulses for the purpose of meeting Federal Communication Commission requirements, cellular telephone and other electronic devices require shielding to inhibit the emission of radiation generated by electronic components and circuitry.

US-PAT-NO: 5717577
DOCUMENT-IDENTIFIER: US 5717577 A

TITLE: Gasketed shield can for shielding emissions of electromagnetic energy

DATE-ISSUED: February 10, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Mendolia; Gregory S.	Forest	VA	N/A	N/A
Roderique; Benjamin O.	Forest	VA	N/A	N/A
Droege; David R.	Lynchburg	VA	N/A	N/A

ABSTRACT:
The present invention places a semi-lossy gasket between a printed circuit board ground pad ring and a metal shield can for shielding electronic components and circuitry which generate electromagnetic radiation. The present invention also provides a variety of means for aligning and mounting the shield can and gasket to the printed circuit board. Guide pins extending from the shield can extend through apertures in the printed circuit board for aligning the shield can to the printed circuit board. The guide pins can be bent or soldered to the printed circuit board and can also include a hooked end for latching on to the printed circuit board.

(3) The present invention pertains in general to the shielding of electronic components and printed circuits, and more particularly, to the use of a gasket constructed from a semi-lossy material and positioned between a shield can and a printed circuit board.

(6)In a first approach, the cellular telephone housing is constructed of a conductive material, either metal or metalized plastic and is used to form all or a part of the conductive capsule. Typically, the housing is made of a front and a rear housing/cover which mate with each other and the printed circuit board to hold the printed circuit board within the two housings. Mating typically occurs along the perimeter of the two housings and the printed circuit board. To inhibit the emission of electromagnetic radiation, a semi-lossy conductive gasket(s) is (are) placed along the perimeter of the two housings to make an electrical contact between the conductive housings and a ground pad ring located along the perimeter of the printed circuit board.

(3) Referring additionally now to FIG. 2A, there is illustrated a cross-sectional view of the printed circuit board 100, of FIG. 1, mounted between a rear portion 170 and a front portion 180 of an electronic device housing. The printed circuit board is constructed of multiple layers and has a ground plane 190 which can be located on any one of the layers of the printed circuit board 100. The ground plane 190 located beneath the electronic components and circuitry 120 is connected to the ground pad ring 100 by means of a via 200. The shield can 210 includes guide pins 220 which extend through the printed circuit board apertures 130. In this embodiment of the present invention, frictional forces created between the surface edges of the shield can guide pins 220, and the inner surface 135 of printed

circuit board apertures 130 hold the shield can 210 to the printed circuit board 100. Alternatively or additionally, the guide pins 220 are soldered 222 to the printed circuit board 100 to provide further structural strength. The guide pins 220 and printed circuit board apertures 130 also align the shield can 210 over the ground pad ring 110 located on the surface of the printed circuit board 100. Sandwiched between the ground pad ring 110 and a lip 230 of the shield can 210, is a conductive semi-lossy gasket 240. The lip 230 of the shield can 210 extends along the entire perimeter of the shield can which also follows and is aligned with the trace of the ground pad ring 110. The semi-lossy conductive gasket 240 extends continuously along the perimeter of the shield can lip 230. An electrically conductive path is created between the shield can 210, the gasket 240, the ground pad ring 110, and the ground plane 190. This conductive path, taken in all three dimensions, creates an electrically conductive capsule surrounding the electronic components and circuitry 120. As electromagnetic radiation is emitted from the electronic components and circuitry 120, the semi-lossy gasket 240 converts a portion of the electromagnetic energy into heat, thereby attenuating the electromagnetic emissions and reducing reflections.

3.The assembly according to claim 1, Barker, III et al. further comprising a heat sink **14** in heat conducting relation with the thermal spreader on a side of the thermal spreader opposite the die.

4. The assembly according to claim 1, Barker, III et al. show wherein the semiconductor die is a microprocessor.

5. The assembly according to claim 1, the combination with Mendolia et al. showing wherein the lossy material of the gasket is a static dissipative material having a volume resistivity of greater than 10^2 ohm cm.

6. The assembly according to claim 5, the combination with Mendolia et al. showing wherein the volume resistivity of the static dissipative material is less than 10^9 ohm cm.

7. The assembly according to claim 1, Barker, III et al. show wherein the gasket is bonded to the substrate with an adhesive **25**.

8. The assembly according to claim 7, Barker, III et al. show wherein the adhesive is conductive.

11. The assembly according to claim 1, the combination with Mendolia et al. showing wherein the gasket has a shielding effectiveness to prevent damage to the die when at least 4 kV of electrostatic discharge pulse is applied to the assembly at a system level in which the assembly is to be used.

12. The assembly according to claim 1, the combination with Mendolia et al. showing wherein the gasket material has a shielding effectiveness of greater than 45 dB tip to 3 GHz in frequency.

23. The electronic package according to claim 22, Barker, III et al. show further comprising a thermal spreader located intermediate the semiconductor die and the heat sink to thermally couple the die and heat sink.

24. The electronic package according to claim 22, the combination with Mendolia et al. showing wherein the lossy material of the gasket is a static dissipative material having, a volume resistivity of greater than 10^2 ohm cm.

27. The combination with Mendolia et al. showing wherein the gasket has a shielding effectiveness to prevent damage to the die when at least 4 kV of electrostatic discharge pulse is applied to the electronic package at a system level in which the electronic package.

28. The combination with Mendolia et al. showing wherein the gasket material has a shielding effectiveness of greater than 45 dB up to 3 GHz.

Therefore, it would have been obvious to one of ordinary skill in the art to use Mendolia et al.'s gasket of lossy conductive material to modify Barker III, et al.'s conductive gasket for the purpose of meeting Federal Communication Commission requirements, cellular telephone and other electronic devices require shielding to inhibit the emission of radiation generated by electronic components and circuitry.

Claims 1 to 8, 10 to 17, 19 to 21 and 23 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Morris (U.S. Patent # 6,507,101 B1) in view of Jensen et al. (U.S. Patent Application Publication # 2003/0037943 A1) and further in view of Alcoe et al. (U.S. Patent Application Publication # 2003/0025180 A1).

1. Morris (figures 1A to 4B) specifically figure 2 show an assembly for packaging and cooling a semiconductor die comprising: a substrate **210**; a semiconductor die **212** mounted on the substrate; and a gasket of a lossy material **202** on the substrate surrounding the die. Jensen et al. show that the gasket can protect the die from electrostatic discharge pulses. Morris/Jensen et al. fails to explicitly show a thermal

spreader in heat conducting relation with the semiconductor die on a side of the die opposite the substrate.

Alcoe et al. is cited for showing an EMI shielding for semiconductor chip carriers. Specifically, Alcoe et al. (figures 1 to 3) specifically figure 2 discloses a thermal spreader **(unlabeled electrically-conductive material between the heat sink 48 and chip 42 and substrate 40)** in heat conducting relation with the semiconductor die on a side of the die opposite the substrate **(see page 3, paragragh [0040])** for the purpose of producing an EMI shield for the structure.

2. The assembly according to claim 1, the combination with Alcoe et al. showing wherein the thermal spreader extends beyond the outer peripheral edge of the die and overhangs an adjacent edge of the gasket **52**.

3.The assembly according to claim 1, the combination with Alcoe et al. further comprising a heat sink **48** in heat conducting relation with the thermal spreader on a side of the thermal spreader opposite the die **42**.

4. The assembly according to claim 1, either show wherein the semiconductor die is a microprocessor.

5. The assembly according to claim 1, either show wherein the lossy material of the gasket is a static dissipative material having a volume resistivity of greater than 10^2 ohm cm.

6. The assembly according to claim 5, either show wherein the volume resistivity of the static dissipative material is less than 10^9 ohm cm.

7. The assembly according to claim 1, the combination with Alcoe et al. showing wherein the gasket is bonded to the substrate with an adhesive **64** (see figure 3).

8. The assembly according to claim 7, the combination with Alcoe et al. showing wherein the adhesive is conductive.

10. The assembly according to claim 1, the combination with Morris show wherein the gasket **204** has a hole therein the size of the die through which the die protrudes.

11. The assembly according to claim 1, either reference show wherein the gasket has a shielding effectiveness to prevent damage to the die when at least 4 kV of electrostatic discharge pulse is applied to the assembly at a system level in which the assembly is to be used.

12. The assembly according to claim 1, either reference show wherein the gasket material has a shielding effectiveness of greater than 45 dB up to 3 GHz in frequency.

13. Morris (figures 1A to 4B) specifically figure 2 show an apparatus for increasing the immunity of a microprocessor form electrostatic discharge events comprising: a substrate **210**; a microprocessor **212** mounted on the substrate; a heat sink **206** in heat conducting relation on a side opposite the microprocessor; a gasket of a lossy material **202** on the substrate surrounding the microprocessor to protect the microprocessor in which Jensen et al. can protect from electrostatic discharge pulses; and a thermal spreader in heat conducting relation with the microprocessor on a side of the microprocessor opposite the substrate; a heat sink **206** in heat conducting relation with the thermal spreader on a side of the thermal spreader opposite the microprocessor; wherein the thermal spreader extends beyond the outer peripheral edge of the microprocessor and overhangs an adjacent edge of the gasket.

Alcoe et al. is cited for showing an EMI shielding for semiconductor chip carriers. Specifically, Alcoe et al. (figures 1 to 3) specifically figure 2 discloses a thermal spreader **(unlabeled electrically-conductive material between the heat sink 48 and chip 42 and substrate 40)** in heat conducting relation with the microprocessor on a side of the microprocessor opposite the substrate; a heat sink **48** in heat conducting relation with the thermal spreader on a side of the thermal spreader opposite the microprocessor; wherein the thermal spreader extends beyond the outer peripheral edge of the microprocessor and overhangs an adjacent edge of the gasket **(see page 3, paragragh [0040])** for the purpose of producing an EMI shield for the structure.

14. The apparatus according to claim 13, either reference show wherein the lossy material of the gasket is a static dissipative material having a volume resistivity of greater than 10^2 ohm cm.

15. The apparatus according to claim 14, either reference show wherein the volume resistivity of the static dissipative material is less than 10^9 ohn cm.

16. The apparatus according to claim 13, the combination with Alcoe et al. showing wherein the gasket is bonded to the substrate with an adhesive **64** (see figure 3).

17. The apparatus according to claim 13, the combination with Morris showing wherein the gasket **202** is the size of the substrate.

19. The apparatus according to claim 13, the combination with Morris showing wherein the gasket has a hole therein the size of the microprocessor through which the microprocessor protrudes.

20. The apparatus according to claim 13, the combination with Morris showing wherein tile gasket has a shielding effectiveness to prevent damage to the

microprocessor when at least 4 kV of electrostatic discharge pulse is applied to the assembly at a system level in which the apparatus is to be used.

21. The apparatus according to claim 13, the combination with Morris showing wherein. tile gasket material has a shielding effectiveness of greater than 45 dB tip to 3 GNz in frequency.

23. The electronic package according to claim 22, the combination with Alcoe et al. further comprising a thermal spreader located intermediate the semiconductor die and the heat sink to thermally couple the die and heat sink.

Therefore, it would have been obvious to one of ordinary skill in the art to use Alcoe et al.'s thermal spreader and Jensen et al.'s EMI/ESD gasket to modify Morris chip to heat sink connection for the purpose of producing an EMI shield for the structure.

Claims 9 and 18 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Morris (U.S. Patent # 6,507,101 B1) in view of Jensen et al. (U.S. Patent Application Publication # 2003/0037943 A1) in view of Alcoe et al. (U.S. Patent Application Publication # 2003/0025180 A1) and further in view of Abe et al. (U. S. Patent # 5,749,586).

Morris, Jensen et al. and Alcoe et al. show the features of the claimed invention as detailed above, but fail to explicitly show wherein the gasket is formed of expanded polytetralluoretliylene material filled with a conductive material to the extent that the gasket material has a volume resistivity of greater than 10^2 ohm cm.

Abe et al. is cited for showing a gasket for sanitary piping. Specifically, Abe et al. (figures 1 to 3) specifically figure 1 discloses a gasket **1** is formed of expanded polytetralluoretliylene material filled with a conductive material to the extent that the gasket material has a volume resistivity of greater than 10^2 ohm cm for the purpose of recovering the sealing function by repeated retightening.

Therefore, it would have been obvious to one of ordinary skill in the art to use Abe et al.'s polytetralluoretliylene gasket to modify Morris/Jensen et al./Alcoe etal.'s gasket for the purpose of recovering the sealing function by repeated retightening.

Claims 9 and 25 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Barker, III et al. (U.S. Patent # 5,175,613) Medolia et al. (U.S. Patent # 5,717,577) and further in view of Abe et al. (U. S. Patent # 5,749,586).

Barker, III et al./ Medolia et al. show the features of the claimed invention as detailed above, but fail to explicitly show wherein the gasket is formed of expanded polytetralluoretliylene material filled with a conductive material to the extent that the gasket material has a volume resistivity of greater than 10^2 ohm cm.

Abe et al. is cited for showing a gasket for sanitary piping. Specifically, Abe et al. (figures 1 to 3) specifically figure 1 discloses a gasket **1** is formed of expanded polytetralluoretliylene material filled with a conductive material to the extent that the gasket material has a volume resistivity of greater than 10^2 ohm cm for the purpose of recovering the sealing function by repeated retightening.

Therefore, it would have been obvious to one of ordinary skill in the art to use Abe et al.'s polytetralluoretliylene gasket and Medolia et al.'s lossy conductive gasket to modify Barker III, et al.'s conductive gasket for the purpose of recovering the sealing function by repeated retightening.

Claim 25 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Morris (U.S. Patent # 6,507,101 B1) in view of Jensen et al. (U.S. Patent Application Publication # 2003/0037943 A1) and further in view of Abe et al. (U. S. Patent # 5,749,586).

Morris/Jensen et al. show the features of the claimed invention as detailed above, but fail to explicitly show wherein the gasket is formed of expanded polytetralluoretliylene material filled with a conductive material to the extent that the gasket material has a volume resistivity of greater than 10^2 ohm cm.

Abe et al. is cited for showing a gasket for sanitary piping. Specifically, Abe et al. (figures 1 to 3) specifically figure 1 discloses a gasket **1** is formed of expanded polytetralluoretliylene material filled with a conductive material to the extent that the gasket material has a volume resistivity of greater than 10^2 ohm cm for the purpose of recovering the sealing function by repeated retightening.

Therefore, it would have been obvious to one of ordinary skill in the art to use Abe et al.'s polytetralluoretliylene gasket to modify Morris/Jensen et al. EMI/ESD gasket for the purpose of recovering the sealing function by repeated retightening.

Response

Applicant's arguments filed 8/2/04 have been fully considered, but are moot in view of the new grounds of rejections detailed above.

The listed references are cited as of interest to this application, but not applied at this time.

Field of Search	Date
U.S. Class and subclass: 257/659,660,706,700,701,712,713,177,675,676,721,790, 921 361/715,704,719,818	2/23/04 10/30/04
Other Documentation: foreign patents and literature in 257/659,660,706,700,701,712,713,177,675,676,721,790, 921 361/715,704,719,818	2/23/04 10/30/04
Electronic data base(s): U.S. Patents EAST	2/23/004 10/30/04

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AOW
10/30/04

Alexander Williams
Primary Examiner